

Technology

- TSMC 40nm G, 0.9/1.8V portable to LP, 1.1/1.8V

Features

- 3.3V IO
- 1.8V IO
- 4kV HBM, 300V MM
- Max. Ratings -0.3 .. 3.9V
- -40 .. 125°C
- TSMC padding compatible

Deliverables

- GDSII
- Abstract (LEF)
- CDL netlist for LVS
- .lib
- Verilog
- Documentation
- Integration guidelines

Status

- Silicon proven

ICS101-3V3IO-T40G is a 1.8V/3.3V capable general purpose digital IO pad based on 1.8V devices

Differentiation

The ICS101-3V3IO-T40G enables the interface between a 40nm ASIC and legacy off chip components or data cards without extra cost of 2.5V/3.3V masks (if available). It provides a reliable, proven and low cost solution for true 3.3V signalling in deep submicron technologies.

The maximum voltage ratings and reliability are superior to overdriven 2.5V IOs in 40nm G/LP.

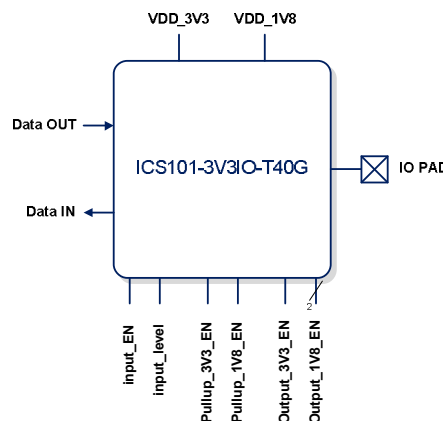
The IP is designed to reliably work under all start-up and power-up scenarios. It uses patented technology to minimize leakage under all conditions up to 125°C. The device can withstand ESD events of over 4kV HBM and 300V MM (ESD design by Sofics™).

The IP is qualified and characterized over corner lots, temperature, high temperature operating life, ESD and LU.

Overview

The ICS101-3V3IO-T40G is complete 1.8V/3.3V capable general purpose digital IO pad. It converts 1.8V internal signalling to 3.3V or 1.8V level input/output while using only 1.8V devices in TSMC 40nm G.

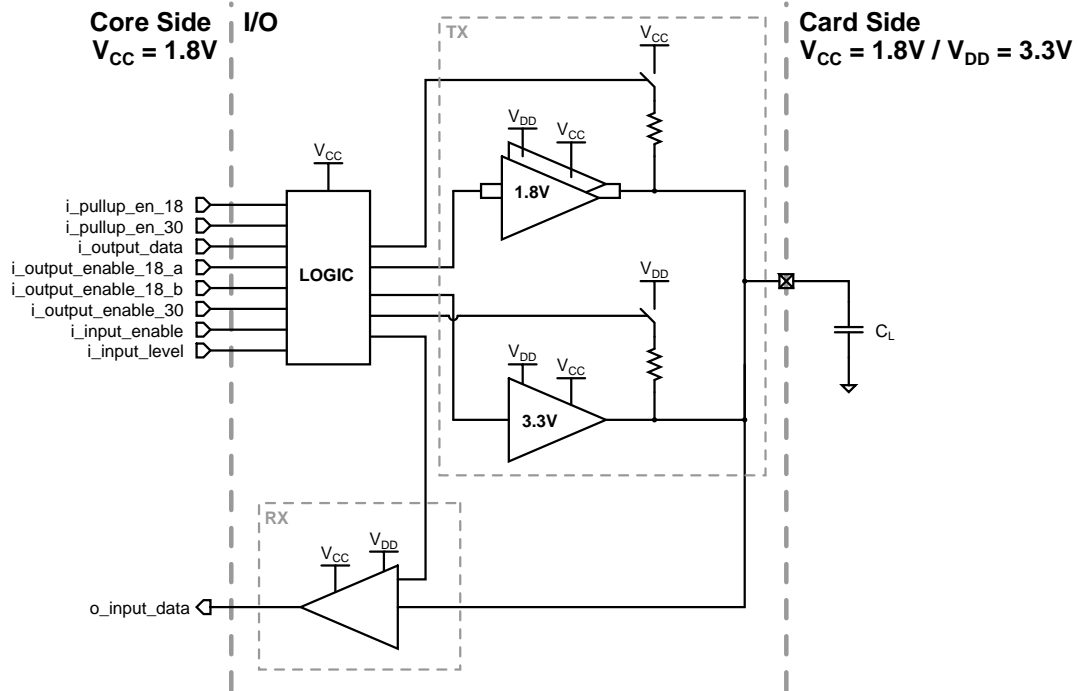
In addition to the IO driver cell(s), the supporting infrastructure is available in the IP: 3.3V power and ground pads; core power and ground pads; isolation cells to the ring. All is compatible with TSMC's tpzn45gsgv18 IO ring. Supporting cells from the TSMC tpzn45gsgv18 IO library can be used, subject to access to this library (not supplied by ICsense).



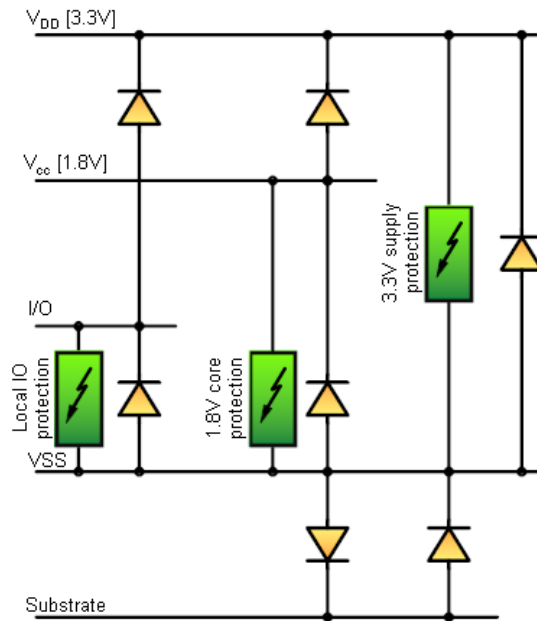
Applications

- SDXC interface
- SIM interface
- MMC interface
- Other 3.3V legacy ASIC-to-card/component interfaces

Functional block Diagram



ESD Block Diagram and ESD characterization



Our service and support

Our service models include:

- Single-use, multi-use, one-time buy-off licensing models for our IP-cores
- Customization or porting of IP-cores to the customers target technology
- Custom development of analog, mixed-signal and high-voltage IP-cores
- Custom ASIC turnkey solutions

In all of these models, we are committed to provide pro-active support from idea to product. We always work closely together with our customers to come to the most optimal solutions for their systems.

About ICsense

ICsense is an ISO 9001:2000 certified IC design house offering analog, mixed-signal and high-voltage IC design services and ASIC turnkey solutions for the automotive, medical, industrial and consumer market.

ICsense provides best-in-class IC design from consultancy and building block/IP design up to complete mixed-signal ASICs or SoCs. Our philosophy is to deliver highly complex, innovative circuits at minimal risks through engineering excellence and close cooperation with our customers. ICsense proudly partners with Sofics and Easics for SoC solutions.

More information on www.icsense.com

About Sofics

Sofics (formerly known as Sarnoff Europe and now independent from Sarnoff Corporation) develops, supports and licenses on-chip ESD design solutions for nano, standard and HV processes. The ESD solutions complement the public, foundry or customer owned protection clamps with focus on low capacitance, low leakage, over voltage tolerant or above standard ESD performance.

Sofics is a TSMC IP Alliance and Design Center Alliance (DCA) partner and UMC IP Alliance partner, and collaborates with Tower Semiconductor for advanced ESD foundry solutions. Sofics and ICsense proudly partner to develop solutions for ICs.

More information on www.sofics.com

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